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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,572	01/23/2004	John Twynam	204552031600	3031
7590	08/01/2005			EXAMINER LEE, EUGENE
Barry E. Bretschneider Morrison & Foerster LLP Suite 300 1650 Tysons Boulevard McLean, VA 22102			ART UNIT 2815	PAPER NUMBER
DATE MAILED: 08/01/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/762,572	TWYNAM, JOHN
	<b>Examiner</b>	<b>Art Unit</b>
	Eugene Lee	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 24 May 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-3 and 5-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-3 and 5-7 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 24 May 2005 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because elements 19, and 14 appear to be pointing to the same layer. According to the amended specification filed 5/24/05, it appears that element 19 is an insulating layer on top of the AlGaN layer 14, however, there does not seem to be any definite structure shown above the AlGaN layer than can be called a separate, insulating layer. The same instance is true for FIG. 4 in regards to element 79, and 74.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. 5,192,987 in view of Inoue et al. 6,639,255 B2. Khan discloses (see, for example, FIG. 5) a transistor (compound semiconductor FET) comprising a buffer layer (AlN layer) 38, substrate 37; a plurality of III-N layers comprising GaN layer 39 and Al<sub>x</sub>Ga<sub>1-x</sub>N layer 41; source contact (source electrode) 43, gate contact (gate electrode) 47, and drain contact (drain electrode) 44. Khan does not disclose an n-type delta doped III-N layer. However, Inoue discloses (see, for example, FIG. 7) a field-effect transistor comprising a buffer layer 702, GaN channel layer 704, and n-type AlGaN electron donor layer (n-type delta doped III-N layer) 703. In column 10, lines 50-57, Inoue discloses the electron donor layer as being doped with Si, and providing electron supply to the channel layer. In column 10, lines 65-67, Inoue discloses that such a structure prevents an increase of the source resistance and reduction of the leakage current. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an n-type delta doped III-N layer in order to prevent an increase of the source resistance and reduce the leakage current.

Regarding the limitation “AlN layer” in line 2 of claim 1, see, for example, column 4, lines 19-20 wherein Khan discloses the buffer layer comprising aluminum nitride (AlN).

Regarding claims 5, and 6, Khan does not disclose each of the semiconductor layers being of a C-plane Ga-surface type. However, Inoue discloses (see, for example, abstract) a semiconductor device comprising layers that have c facets of Ga atoms (C-plane Ga-surface type). In column 10, lines 65-67, Inoue discloses that such a structure prevents an increase of the source resistance and reduction of the leakage current. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have each of the semiconductor layers being of a C-plane Ga-surface type in order to prevent an increase of the source resistance and reduce the leakage current.

Regarding the limitation “substrate is sapphire” in line 2 of claim 5, see, for example, column 2, lines 41-43, wherein Khan discloses the material of the substrate being sapphire.

Regarding lines 5-6 of claim 5, Khan in view of Inoue does not disclose the sheet doping concentration of the n-type delta doped III-N layer being within a range of  $1 \times 10^{13} \text{ cm}^{-2}$  to  $2 \times 10^{13} \text{ cm}^{-2}$ . However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the sheet doping concentration of a n-type delta doped III-N layer in order to achieve a low resistance value and high withstand voltage properties. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have sheet doping concentration of the n-type delta doped III-N layer is within a range of  $1 \times 10^{13} \text{ cm}^{-2}$  to  $2 \times 10^{13} \text{ cm}^{-2}$  because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the sheet doping concentration in order to achieve a low resistance value and high withstand voltage properties.

See *In re Aller*, 105 USPQ 233.

Regarding the limitation “substrate is SiC” in line 2 of claim 6, see, for example, column 6, lines 7-10, wherein Khan discloses the material of the substrate being silicon carbide (SiC).

Regarding lines 5-6 of claim 6, Khan in view of Inoue does not disclose the sheet doping concentration of the n-type delta doped III-N layer being within a range of  $5 \times 10^{12} \text{ cm}^{-2}$  to  $1.5 \times 10^{13} \text{ cm}^{-2}$ . However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the sheet doping concentration of a n-type delta doped III-N layer in order to achieve a low resistance value and high withstand voltage properties. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have sheet doping concentration of the n-type delta doped III-N layer is within a range of  $5 \times 10^{12} \text{ cm}^{-2}$  to  $1.5 \times 10^{13} \text{ cm}^{-2}$  because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the sheet doping concentration in order to achieve a low resistance value and high withstand voltage properties.

See *In re Aller*, 105 USPQ 233.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. ‘987 in view of Inoue et al. ‘255 B2 as applied to claims 1, 2, 5, and 6 above, and further in view of Phillips 6,770,902 B2. Khan in view of Inoue does not disclose an insulating layer. However, Phillips discloses (see, for example, figure) a transistor comprising a gate insulation layer 32. In column 5, lines 58-65, Phillips discloses that the gate insulation layer forms a MISFET instead of a Schottky contact. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an insulating layer in order to form another semiconductor device such as a MISFET (instead of a Schottky contact).

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5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. '987 in view of Inoue et al. '255 B2 as applied to claims 1, 2, 5, and 6 above, and further in view of Abrokwah et al. 5,895,929. Khan in view of Inoue does not disclose an electronic circuit provided with the compound semiconductor FET. However, Abrokwah discloses (see, for example, column 1, lines 15-46) FETS being part of electronic circuits such as logic and control circuits, high speed digital circuits, and the like. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an electronic circuit provided with the compound semiconductor FET in order to integrate the transistors in more robust devices.

*Response to Arguments*

6. Applicant's arguments with respect to claims 1-3, and 5-7 have been considered but are moot in view of the new ground(s) of rejection.

*Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

#### **INFORMATION ON HOW TO CONTACT THE USPTO**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee  
July 28, 2005

